Fig. 1
(PRIOR ART)

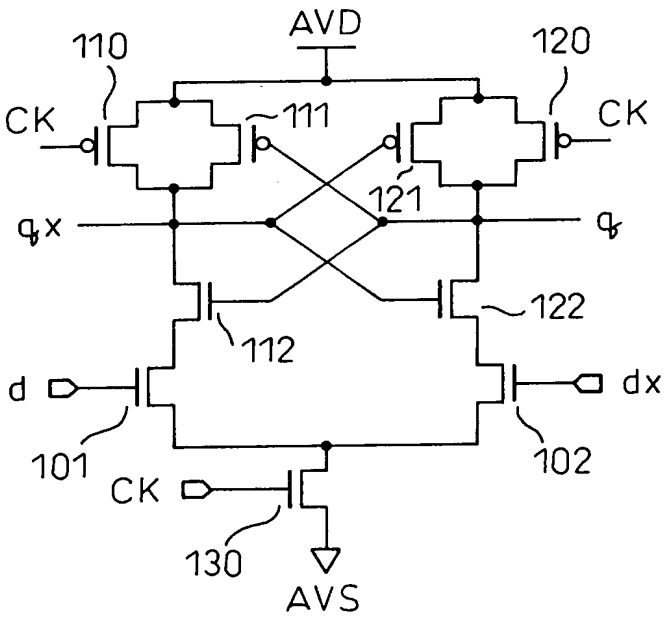


Fig.2

(PRIOR ART)

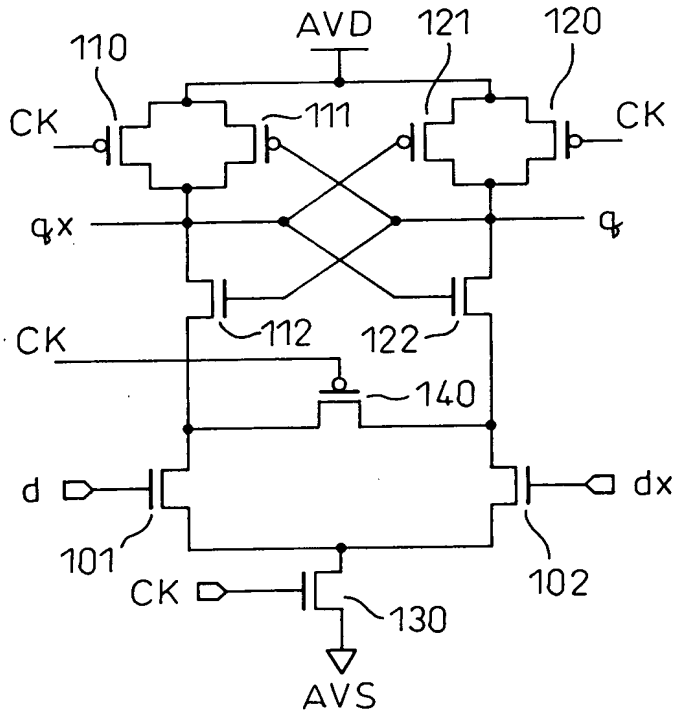


Fig.3
(PRIOR ART)

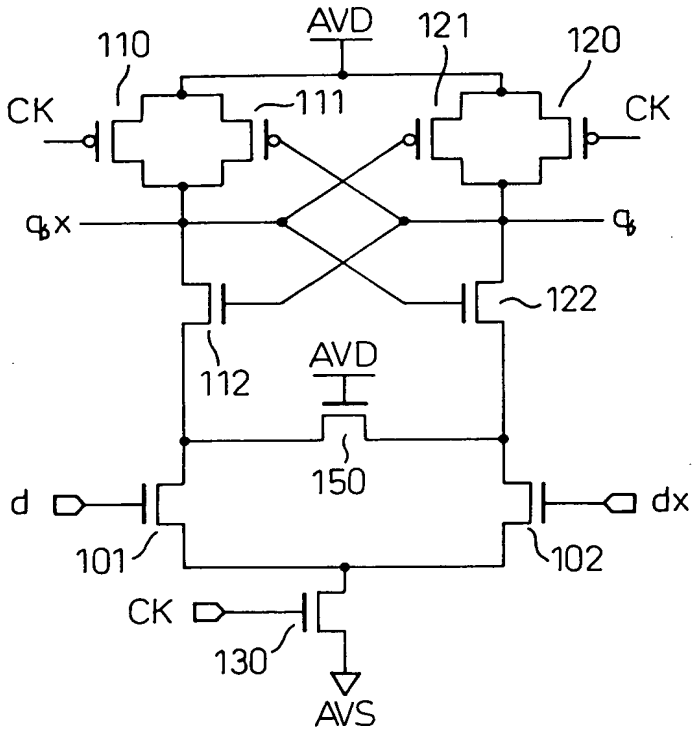


Fig.4

(PRIOR ART)

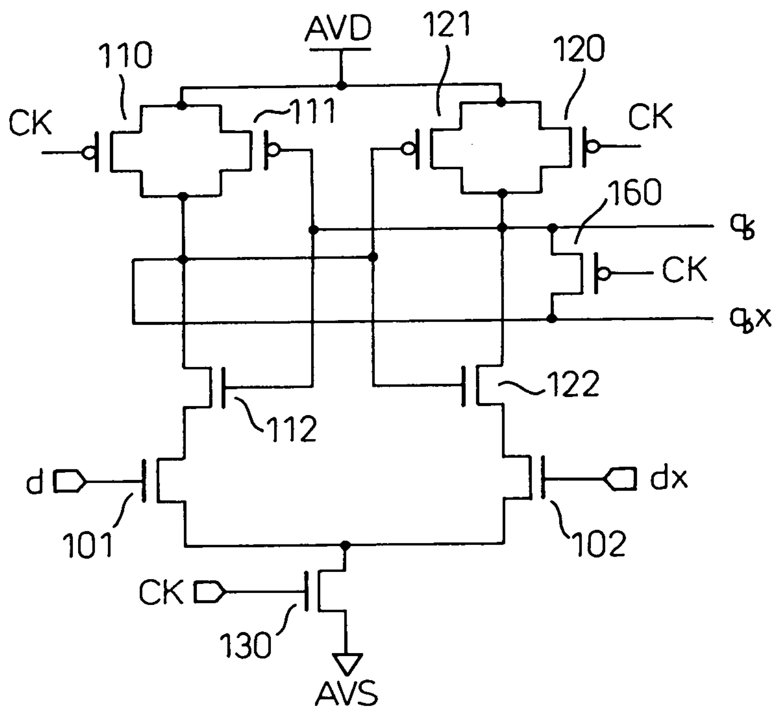


Fig.5

(PRIOR ART)

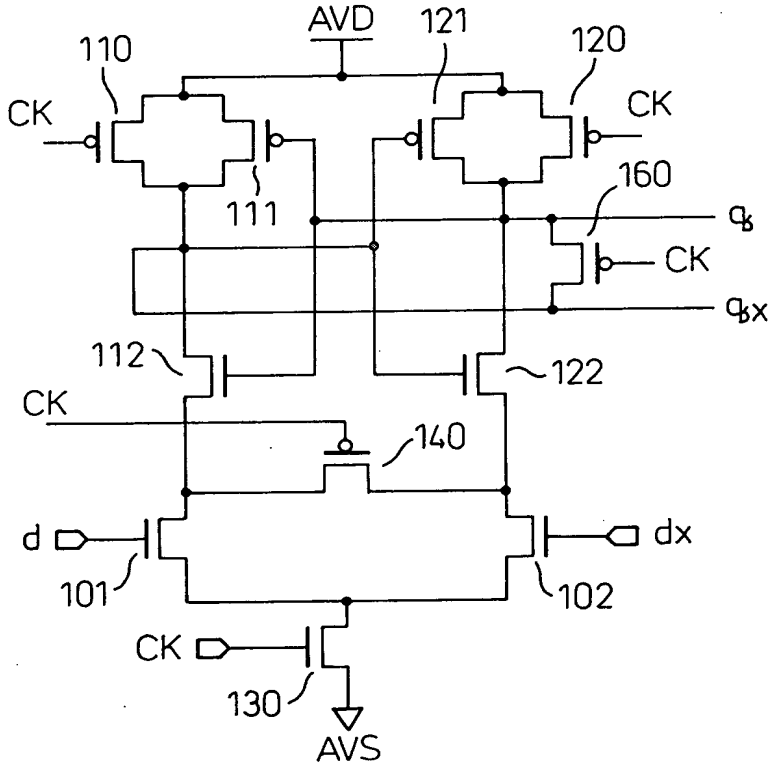


Fig.6

(PRIOR ART)

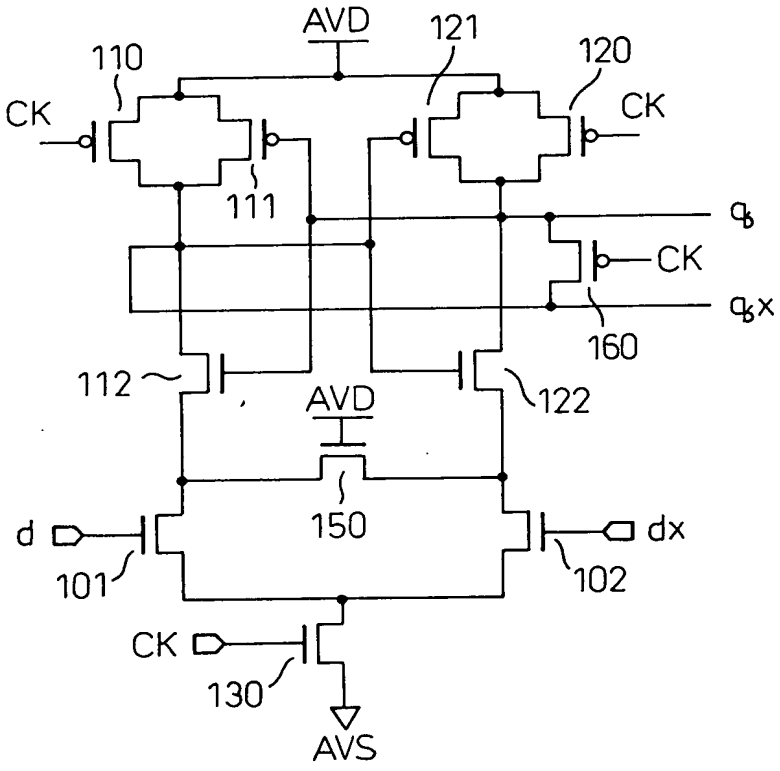


Fig. 7

(PRIOR ART)

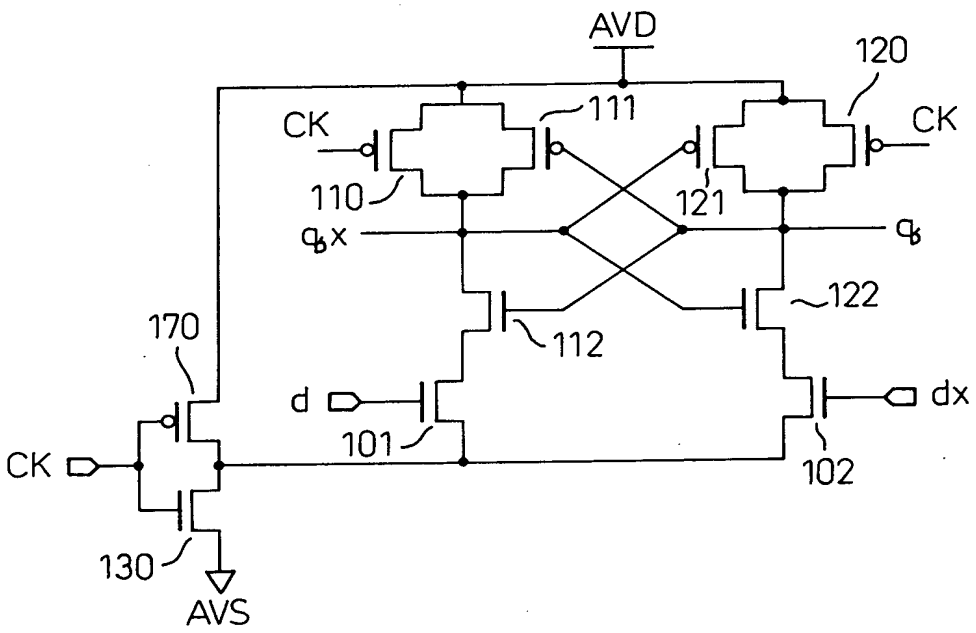


Fig.8

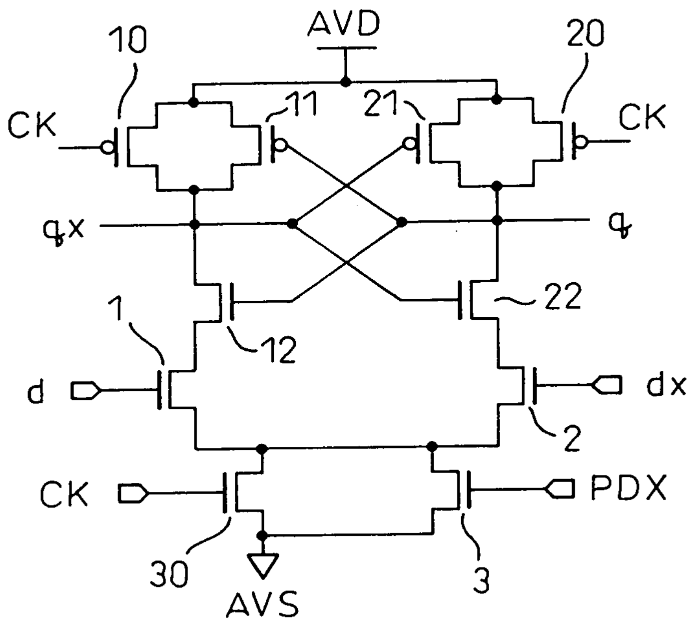


Fig.9

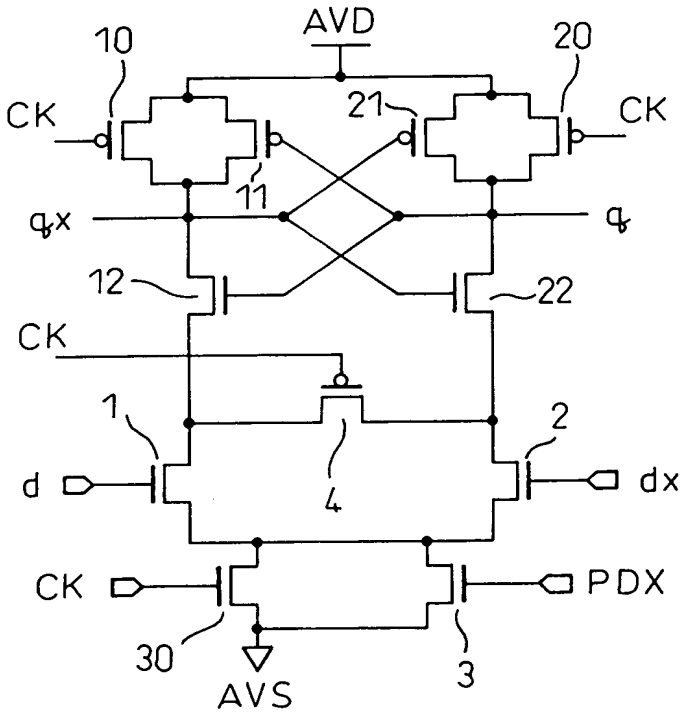


Fig.10

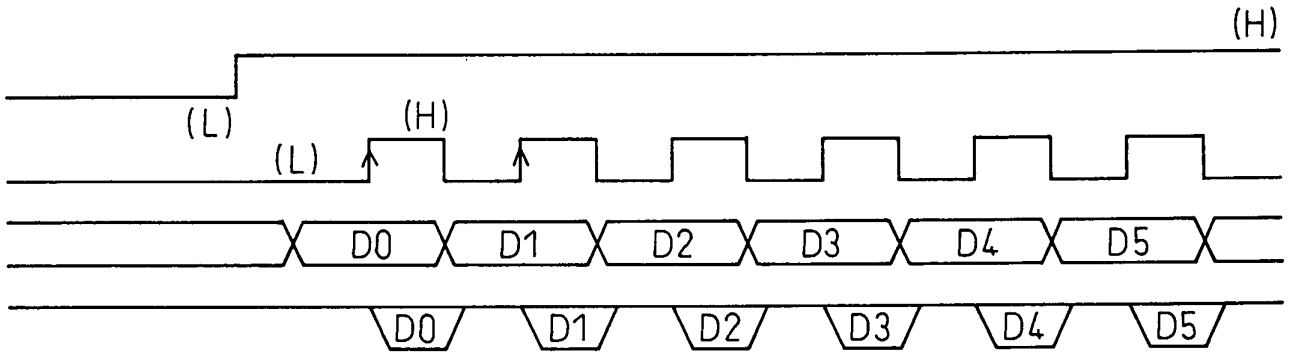


Fig.11A

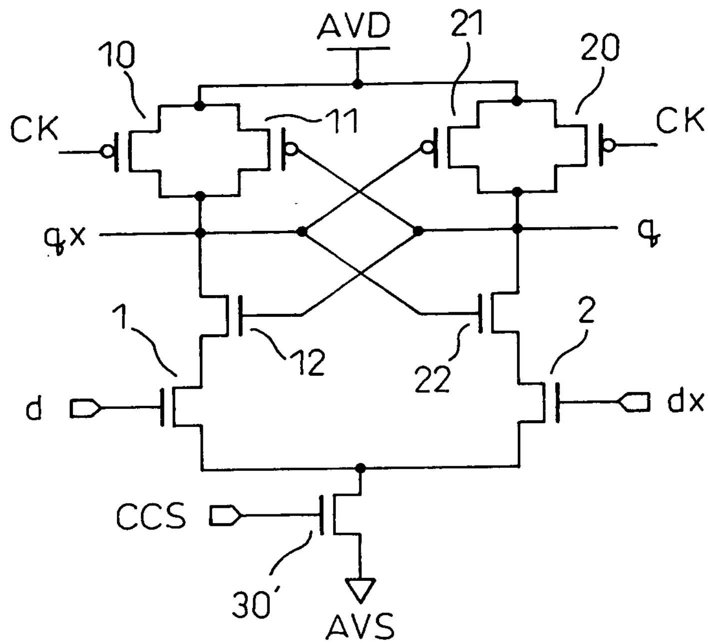


Fig.11B

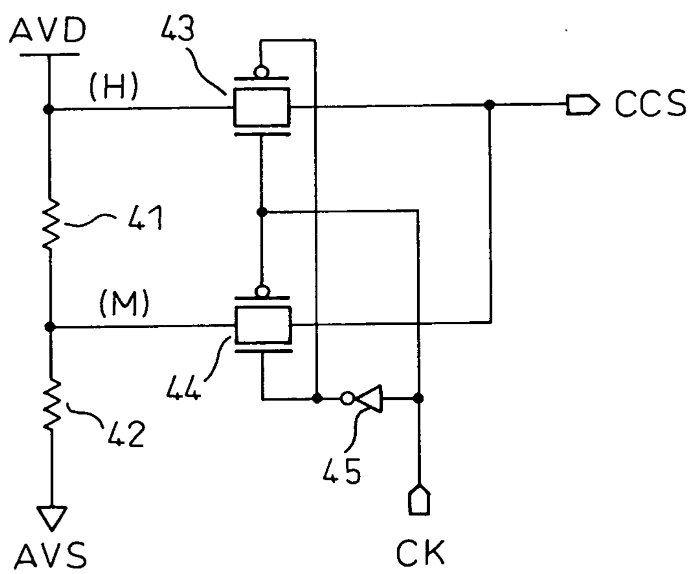


Fig.12

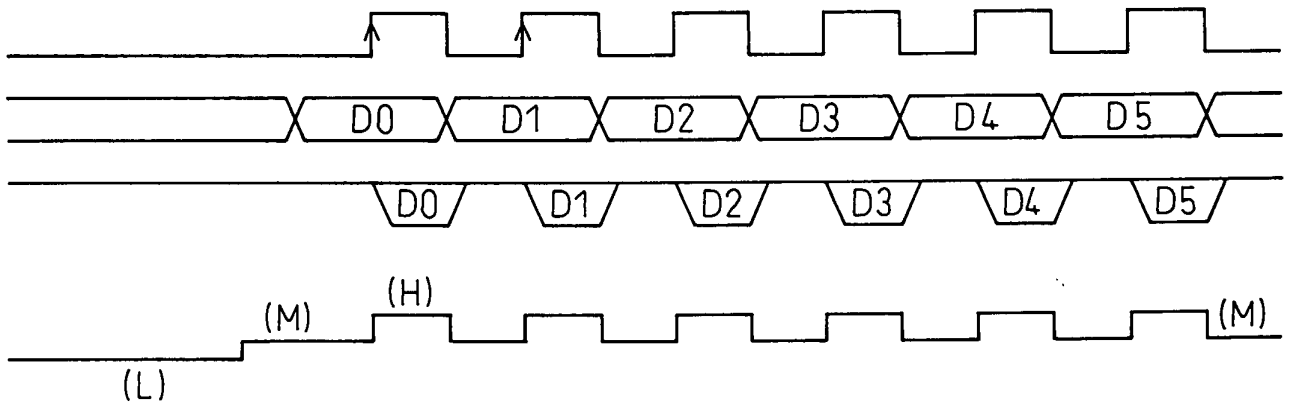


Fig.13

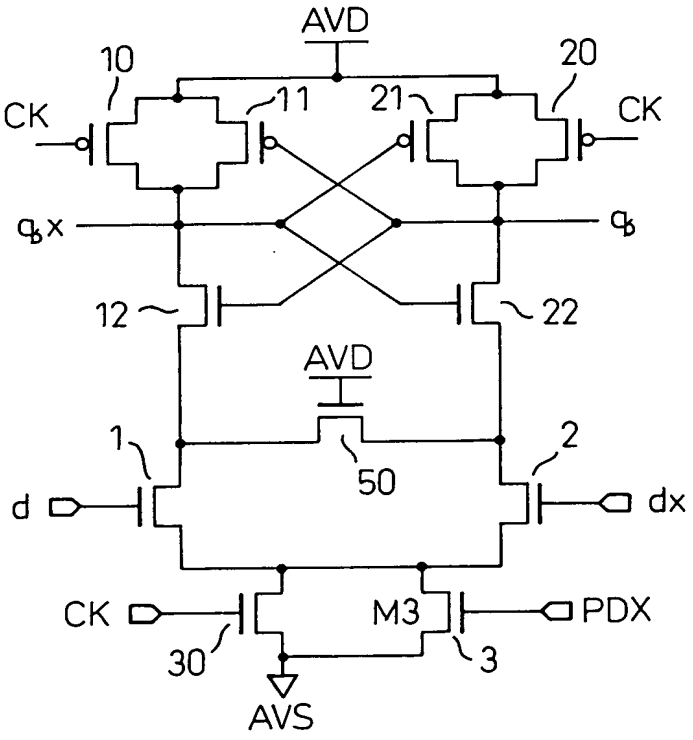


Fig.14

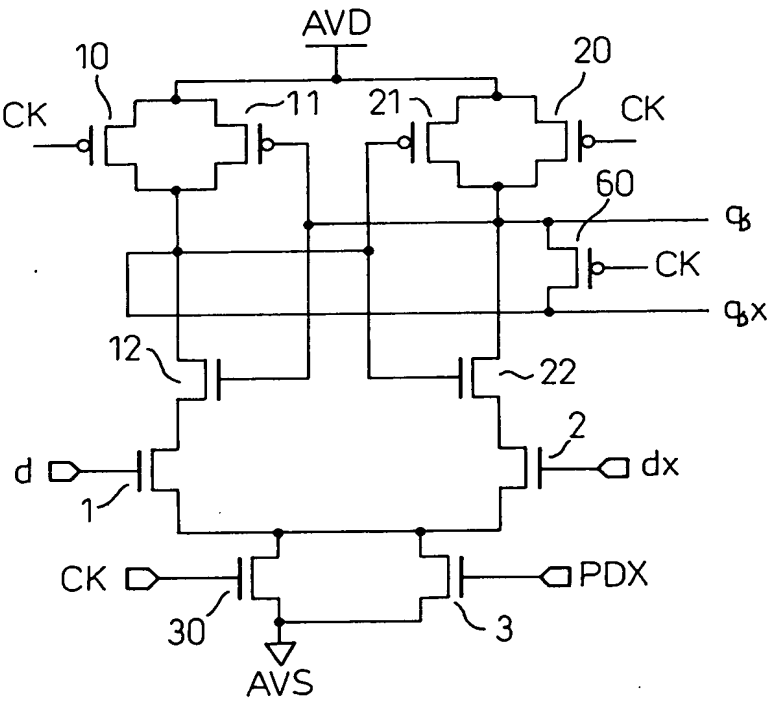


Fig.15

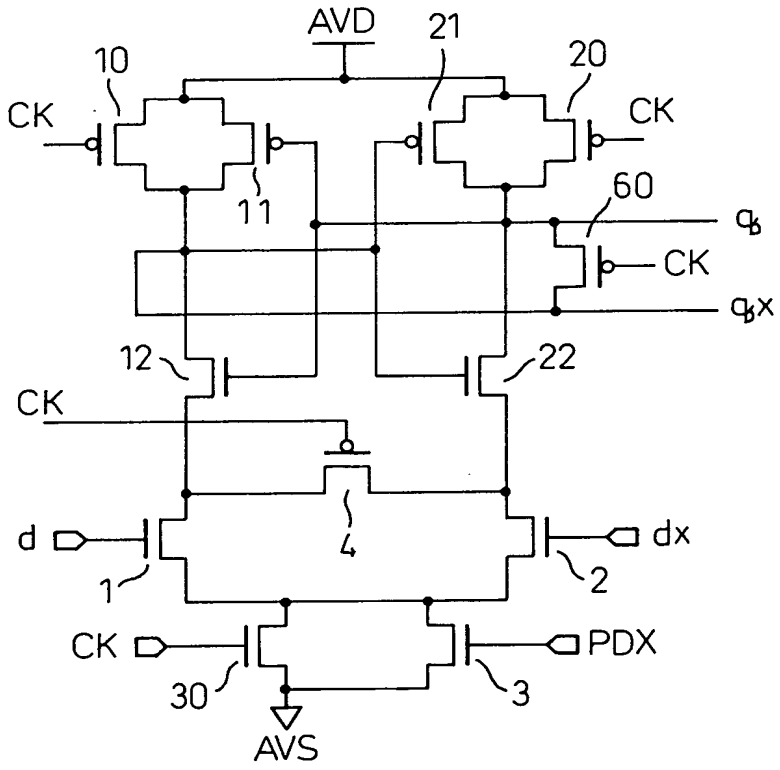


Fig.16

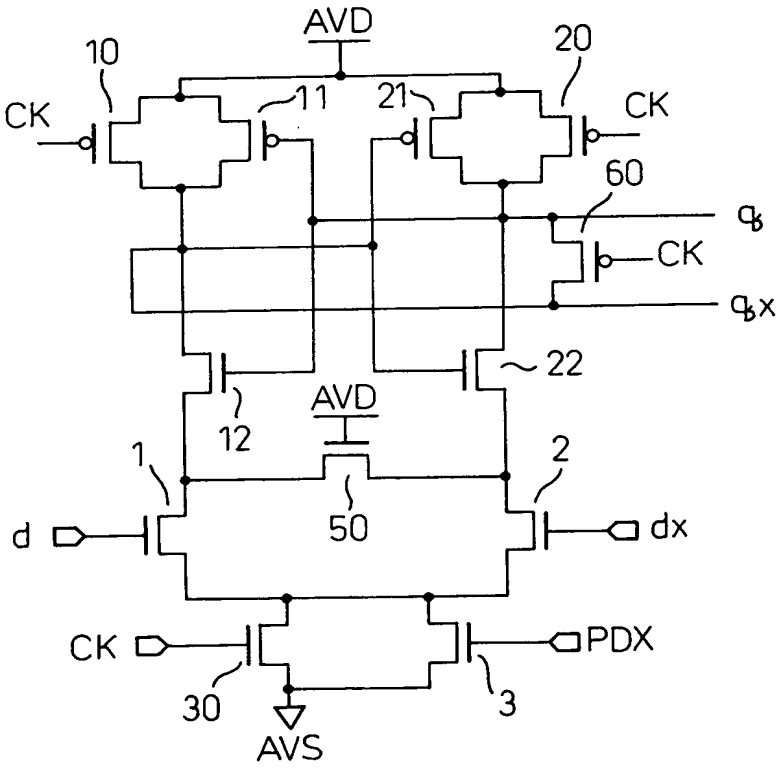


Fig.17

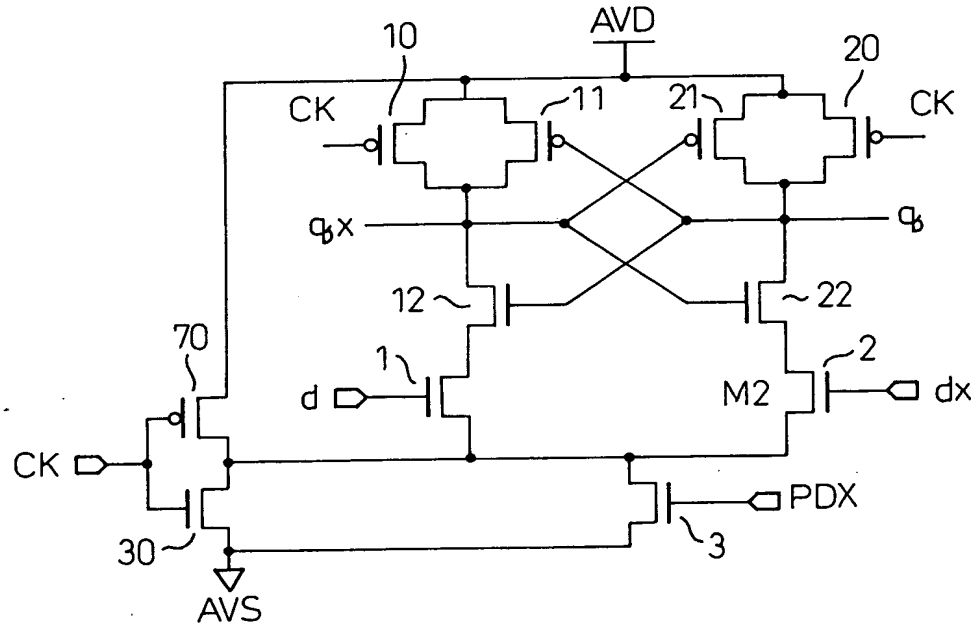


Fig. 18

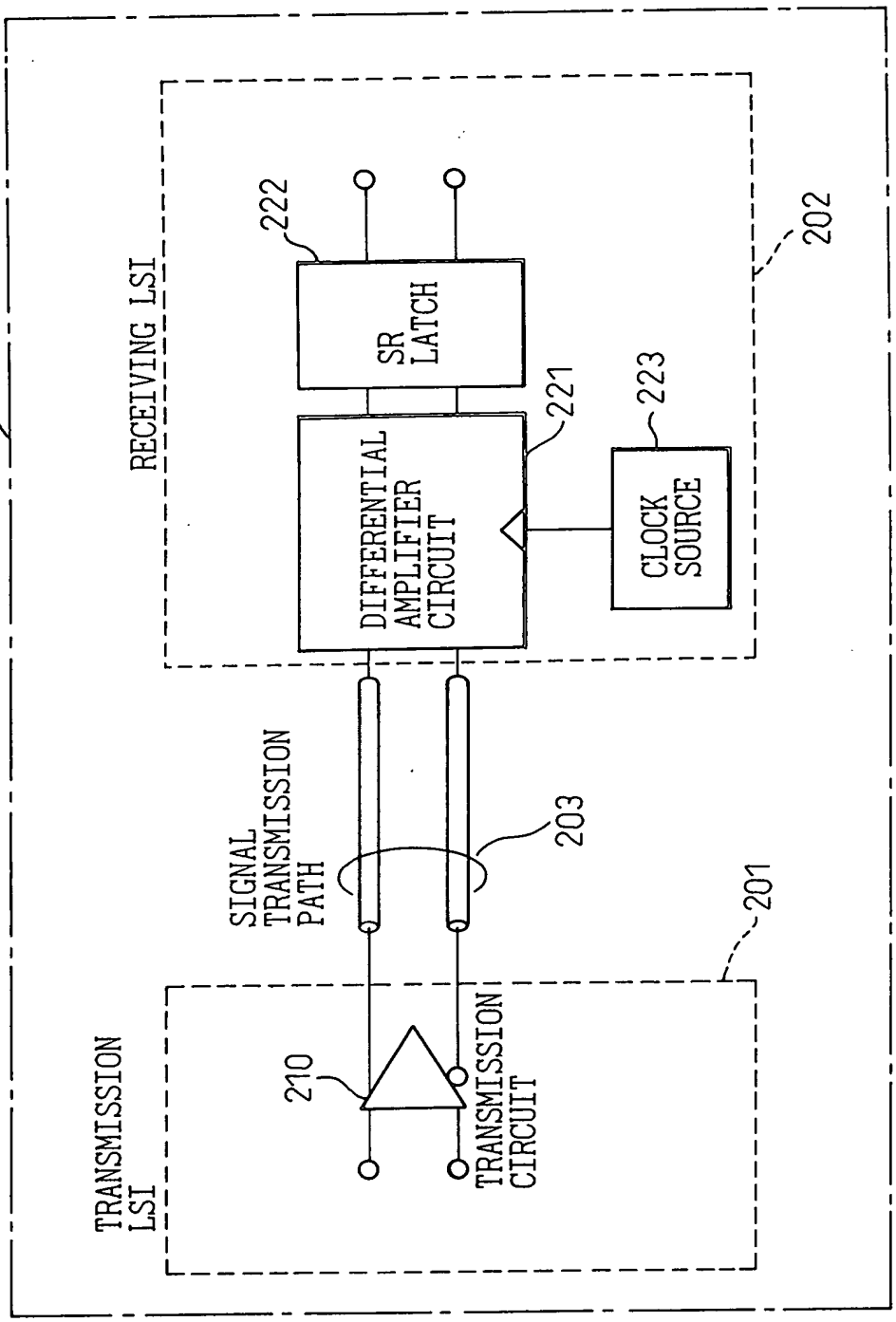
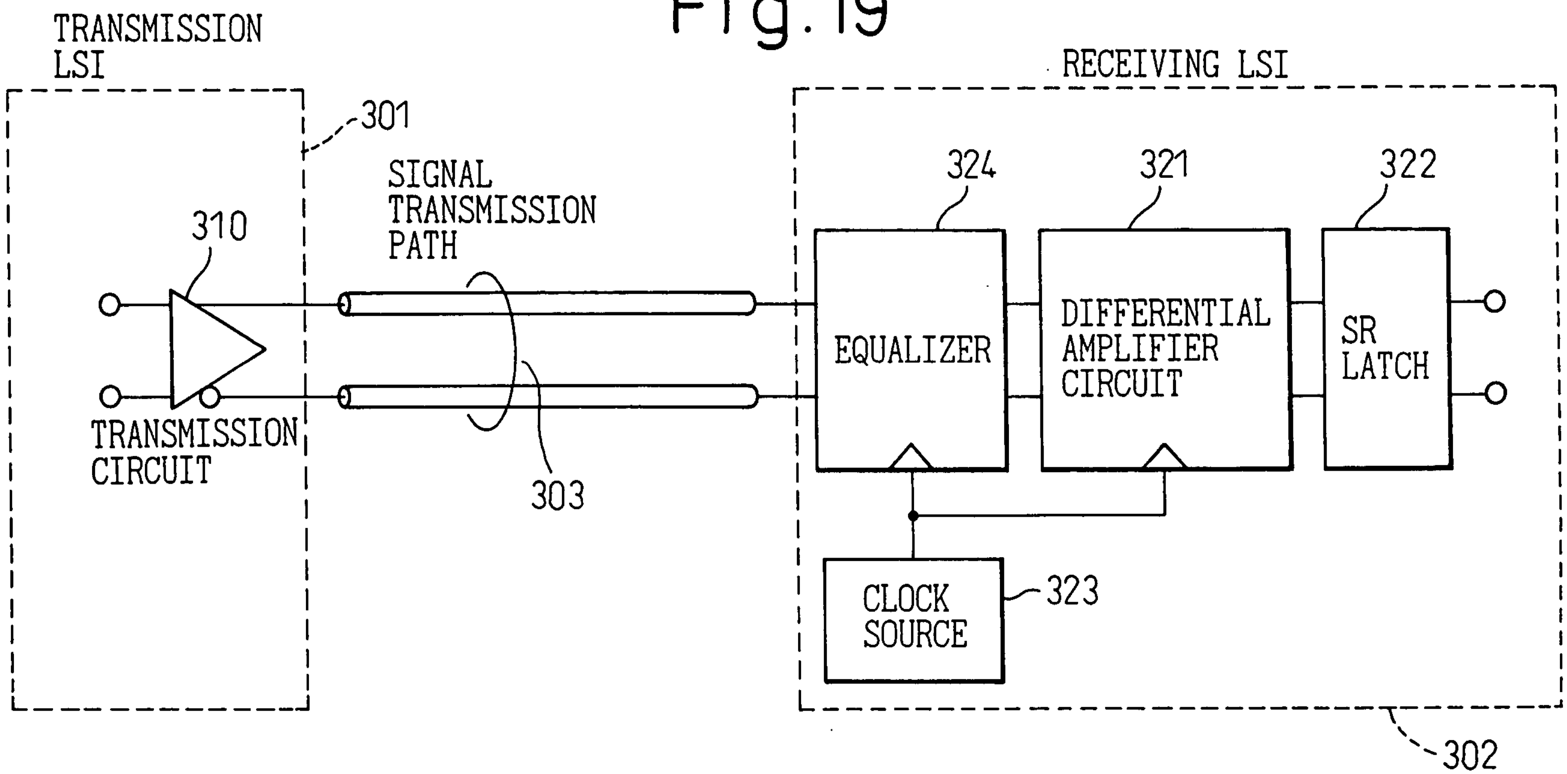


Fig.19



TRANSMISSION LSI
301
310
TRANSMISSION CIRCUIT
SIGNAL TRANSMISSION PATH
303
RECEIVING LSI
324
EQUALIZER
321
DIFFERENTIAL AMPLIFIER CIRCUIT
322
SR LATCH
CLOCK SOURCE
323
302

Fig.20

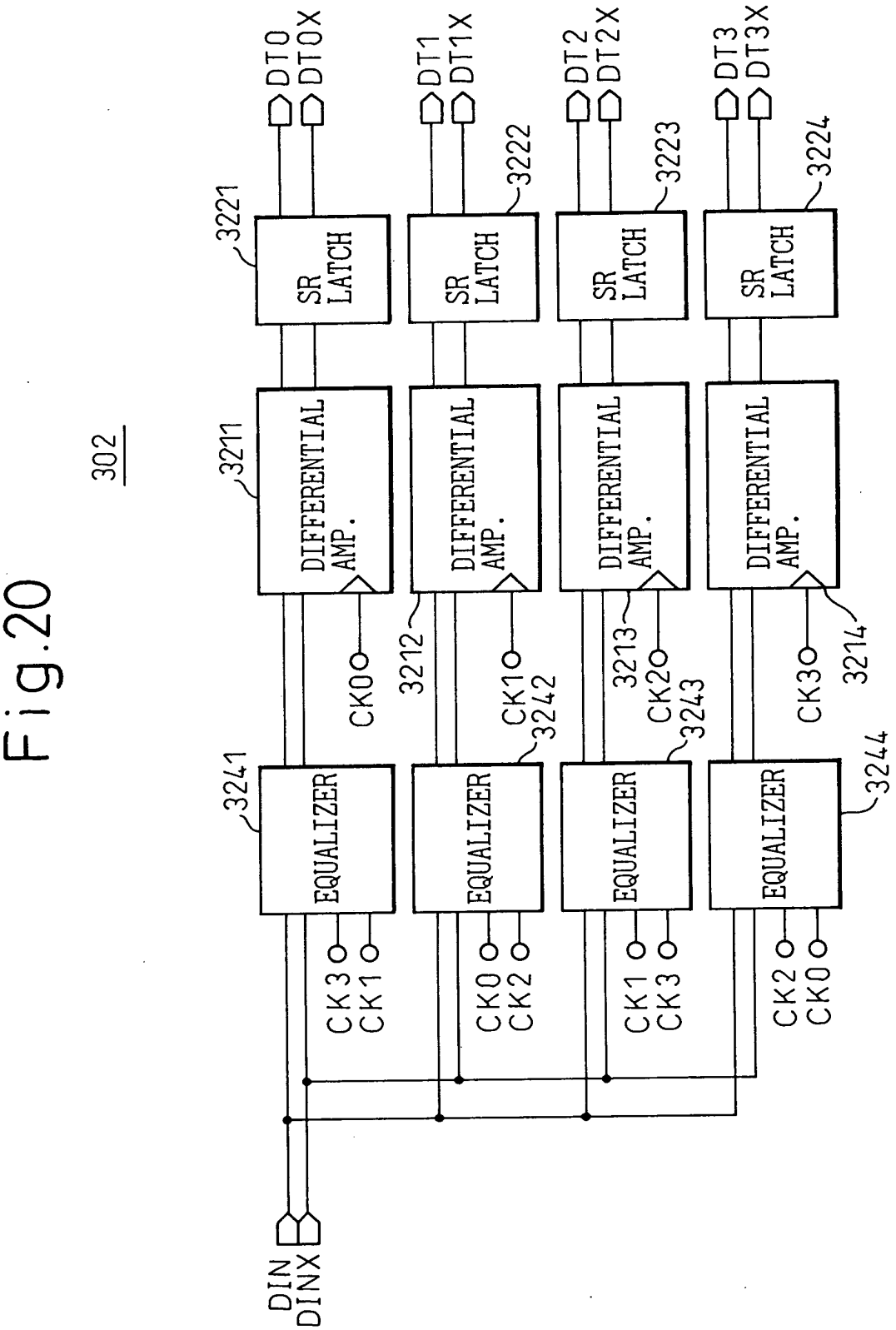

302
DT0
DT0X
DT1
DT1X
DT2
DT2X
DT3
DT3X
3221
3222
3223
3224
SR LATCH
SR LATCH
SR LATCH
SR LATCH
3211
DIFFERENTIAL AMP.
DIFFERENTIAL AMP.
DIFFERENTIAL AMP.
DIFFERENTIAL AMP.
3212
3213
3214
CK0
CK1
CK2
CK3
3241
3242
3243
3244
EQUALIZER
EQUALIZER
EQUALIZER
EQUALIZER
CK3
CK1
CK0
CK2
CK1
CK3
CK2
CK0
DIN
DINX

Fig.21

3241

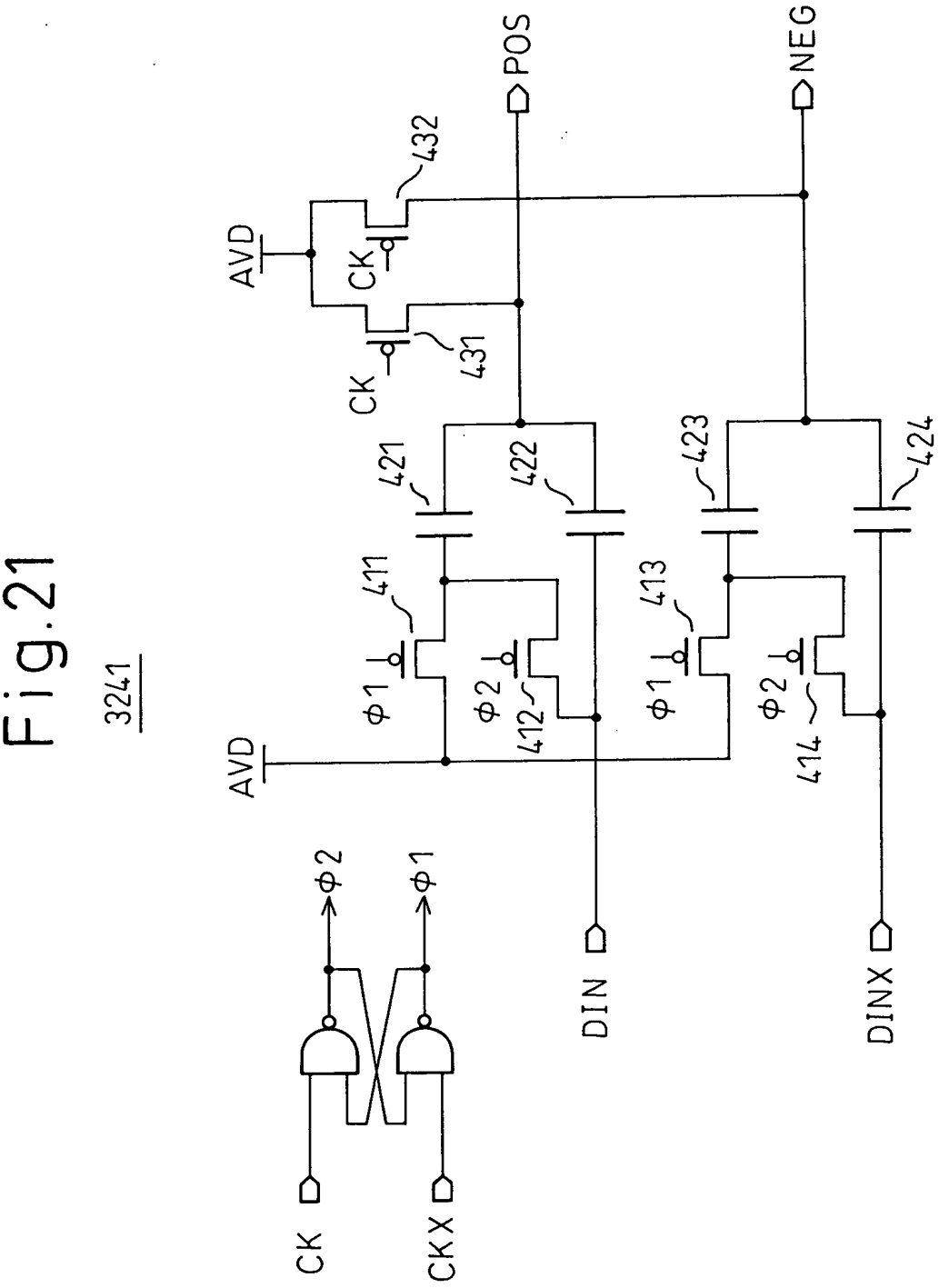


Fig.22

3221

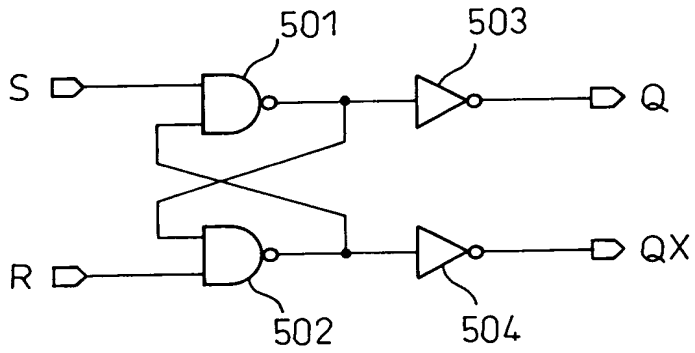


Fig.23

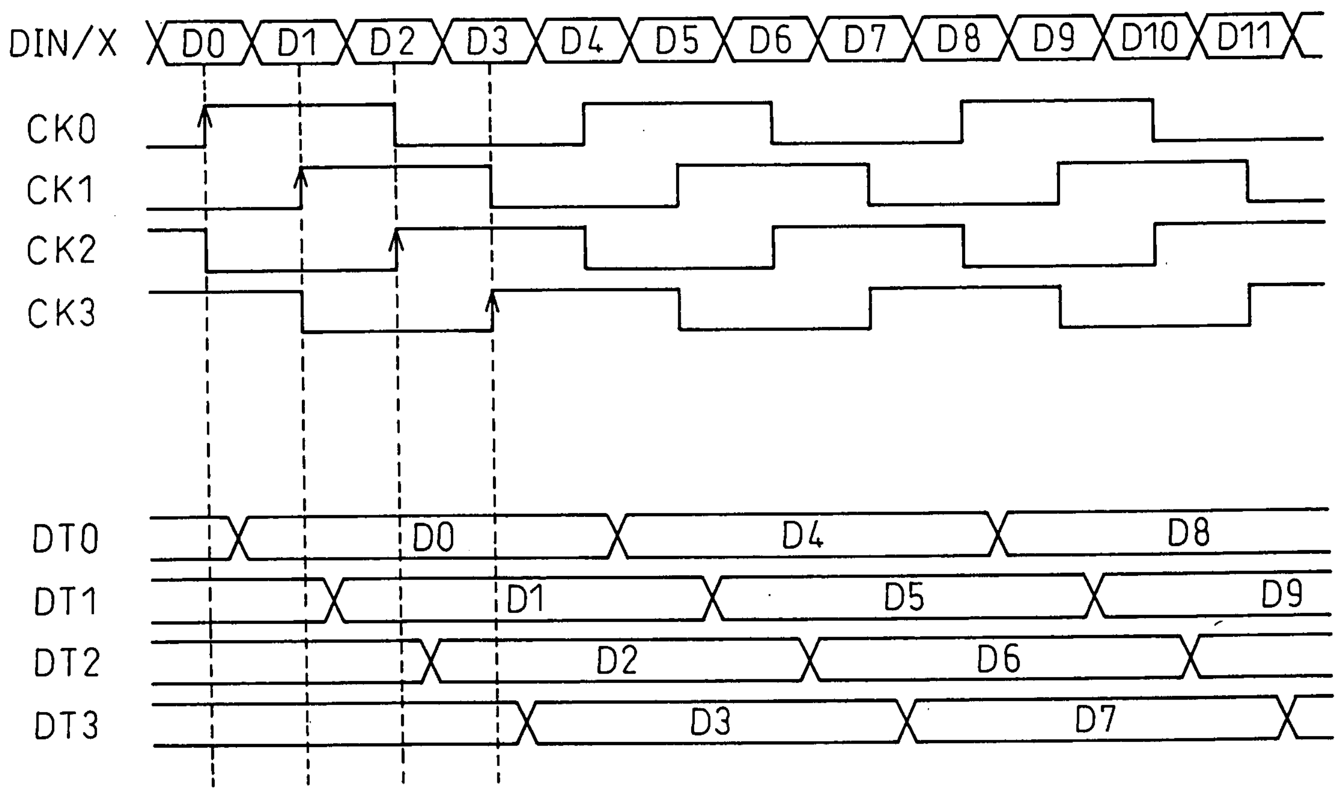

DIN/X
D0
D1
D2
D3
D4
D5
D6
D7
D8
D9
D10
D11
CK0
CK1
CK2
CK3
DT0
DT1
DT2
DT3
D0
D4
D8
D1
D5
D9
D2
D6
D3
D7

Fig.24

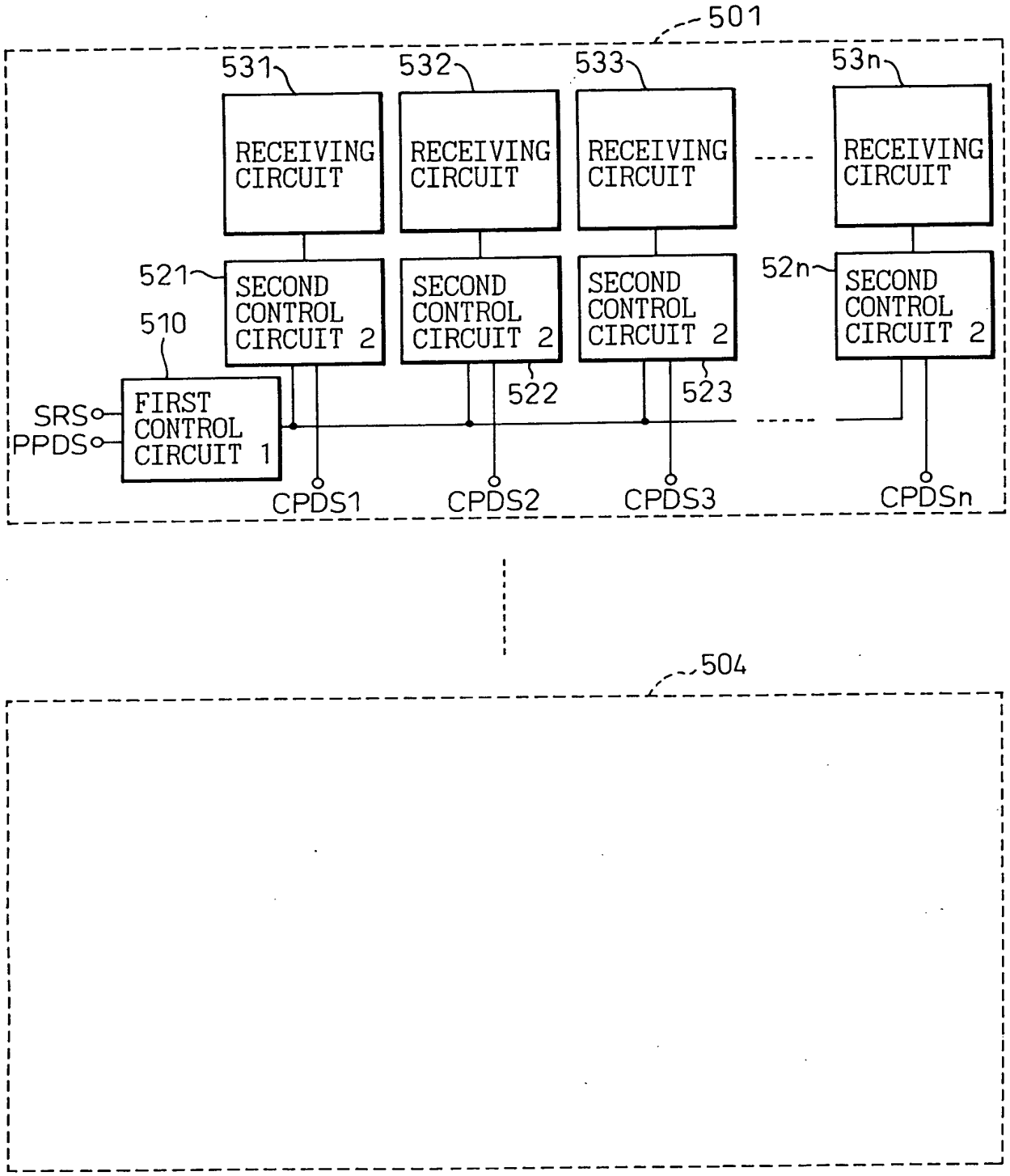

501
531
532
533
53n
RECEIVING CIRCUIT
RECEIVING CIRCUIT
RECEIVING CIRCUIT
RECEIVING CIRCUIT
521
52n
SECOND CONTROL CIRCUIT 2
SECOND CONTROL CIRCUIT 2
SECOND CONTROL CIRCUIT 2
SECOND CONTROL CIRCUIT 2
510
522
523
SRS
PPDS
FIRST CONTROL CIRCUIT 1
CPDS1
CPDS2
CPDS3
CPDSn
504

Fig.25A

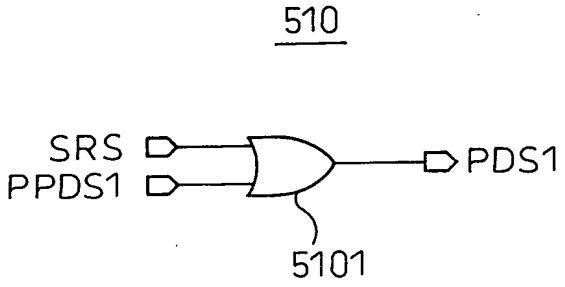


Fig.25B